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Integration of Barrier Layer and Seed Layer

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Integration of Barrier Layer and Seed Layer

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention generally relates to an apparatus and method of depositing a barrier layer and a seed layer over the barrier layer. More particularly, the present invention relates to an apparatus and method of depositing a barrier layer and depositing a seed layer comprising copper and another metal over the barrier layer.

Description of the Related Art

[0002] Reliably producing sub-micron and smaller features is one of the key technologies for the next generation of very large scale integration (VLSI) and ultra large scale integration (ULSI) of semiconductor devices. However, as the fringes of circuit technology are pressed, the shrinking dimensions of interconnects in VLSI and ULSI technology have placed additional demands on the processing capabilities. The multilevel interconnects that lie at the heart of this technology require precise processing of high aspect ratio features, such as vias and other interconnects. Reliable formation of these interconnects is very important to VLSI and ULSI success and to the continued effort to increase circuit density and quality of individual substrates.

[0003] As circuit densities increase, the widths of vias, contacts and other features, as well as the dielectric materials between them, decrease to sub-micron dimensions (e.g., less than 0.20 micrometers or less), whereas the thickness of the dielectric layers remains substantially constant, with the result that the aspect ratios for the features, *i.e.*, their height divided by width, increase. Many traditional deposition processes have difficulty filling sub-micron structures where the aspect ratio exceeds 4:1, and particularly where the aspect ratio exceeds 10:1. Therefore, there is a great amount of ongoing effort being directed at the formation of substantially void-free and seam-free sub-micron features having high aspect ratios.

[0004] Currently, copper and its alloys have become the metals of choice for sub-micron interconnect technology because copper has a lower resistivity than aluminum, (1.7 $\mu\Omega$-cm compared to 3.1 $\mu\Omega$-cm for aluminum), and a higher current carrying capacity and significantly higher electromigration resistance. These characteristics are

important for supporting the higher current densities experienced at high levels of integration and increased device speed. Further, copper has a good thermal conductivity and is available in a highly pure state.

[0005] Copper metallization can be achieved by a variety of techniques. A typical method generally comprises physical vapor depositing a barrier layer over a feature, physical vapor depositing a copper seed layer over the barrier layer, and then electroplating a copper conductive material layer over the copper seed layer to fill the feature. Finally, the deposited layers and the dielectric layers are planarized, such as by chemical mechanical polishing (CMP), to define a conductive interconnect feature.

[0006] However, one problem with the use of copper is that copper diffuses into silicon, silicon dioxide, and other dielectric materials which may compromise the integrity of devices. Therefore, conformal barrier layers become increasingly important to prevent copper diffusion. Tantalum nitride has been used as a barrier material to prevent the diffusion of copper into underlying layers. One problem with prior uses of tantalum nitride and other barrier layers, however, is that these barrier layers are poor wetting agents for the deposition of copper thereon which may cause numerous problems. For example, during deposition of a copper seed layer over these barrier layers, the copper seed layer may agglomerate and become discontinuous, which may prevent uniform deposition of a copper conductive material layer (i.e. electroplating of a copper layer) over the copper seed layer. In another example, subsequent processing at high temperatures of a substrate structure having a copper layer deposited over these barrier layers may cause dewetting and the formation of voids in the copper layer. In still another example, thermal stressing of formed devices through use of the devices may cause the generation of voids in the copper layer and device failure. Thus, there is a need for an improved interconnect structure and method of depositing the interconnect structure.

SUMMARY OF THE INVENTION

[0007] The present invention generally relates to filling of a feature by depositing a barrier layer, depositing a seed layer over the barrier layer, and depositing a conductive layer over the seed layer. In one embodiment, the seed layer comprises a copper alloy seed layer deposited over the barrier layer. For example, the copper alloy seed layer may comprise copper and a metal, such as aluminum, magnesium, titanium, zirconium,

tin, and combinations thereof. In another embodiment, the seed layer comprises a copper allloy seed layer deposited over the barrier layer and a second seed layer deposited over the copper alloy seed layer. The copper alloy seed layer may comprise copper and a metal, such as aluminum, magnesium, titanium, zirconium, tin, and combinations thereof of. The second seed layer may comprise a metal, such as undoped copper. In still another embodiment, the seed layer comprises a first seed layer and a second seed layer. The first seed layer may comprise a metal, such as aluminum, magnesium, titanium, zirconium, tin, and combinations thereof. The second seed layer may comprise a metal, such as undoped copper.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] So that the manner in which the above recited features, advantages and objects of the present invention are attained and can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to the embodiments thereof which are illustrated in the appended drawings.

[0009] It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[0010] Figure 1 is a schematic cross-sectional view of one embodiment of a processing system that may be used to form one or more barrier layers by atomic layer deposition.

[0011] Figure 2A is a schematic cross-sectional view of one embodiment of a substrate having a dielectric layer deposited thereon.

[0012] Figure 2B is a schematic cross-sectional view of one embodiment of a barrier layer formed over the substrate structure of Figure 2A.

[0013] Figures 3A-C illustrate one embodiment of alternating chemisorption of monolayers of a tantalum containing compound and a nitrogen containing compound on a portion of substrate at a stage of barrier layer formation.

[0014] Figure 4 is a schematic cross-sectional view of one embodiment of a process system capable of physical vapor deposition which may be used to deposit a copper alloy seed layer.

[0015] Figures 5A-C are schematic cross-sectional views of embodiments of depositing a seed layer over a barrier layer of Figure 2B.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Process Chamber Adapted for Depositing a Barrier Layer

[0016] Figure 1 is a schematic cross-sectional view of one exemplary embodiment of a processing system 10 that may be used to form one or more barrier layers by atomic layer deposition in accordance with aspects of the present invention. Of course, other processing systems may also be used.

[0017] The process system 10 generally includes a process chamber 100, a gas panel 130, a control unit 110, a power supply 106, and a vacuum pump 102. The process chamber 100 generally houses a support pedestal 150, which is used to support a substrate such as a semiconductor wafer 190 within the process chamber 100.

[0018] In the chamber 100, the support pedestal 150 may be heated by an embedded heating element 170. For example, the pedestal 150 may be resistively heated by applying an electric current from an AC power supply to the heating element 170. The wafer 190 is, in turn, heated by the pedestal 150, and may be maintained within a desired process temperature range, for example, between about 20°C and about 1000°C depending on the specific process.

[0019] A temperature sensor 172, such as a thermocouple, may be embedded in the wafer support pedestal 150 to monitor the pedestal temperature. For example, the measured temperature may be used in a feedback loop to control electric current applied to the heating element 170 from the power supply 106, such that the wafer temperature can be maintained or controlled at a desired temperature or within a desired temperature range suitable for a certain process application. The pedestal 150 may also be heated using radiant heat (not shown) or other heating methods.

[0020] The vacuum pump 102 may be used to evacuate process gases from the process chamber 100 and may be used to help maintain a desired pressure or desired pressure within a pressure range inside the chamber 100. An orifice 120 through a wall of the chamber 100 is used to introduce process gases into the process chamber 100. The size of the orifice 120 conventionally depends on the size of the process chamber 100.

[0021] The orifice 120 is coupled to the gas panel 130 in part by a valve 125. The gas panel 130 may be configured to receive and then provide a resultant process gas from

two or more gas sources 135, 136 to the process chamber 100 through the orifice 120 and the valve 125. The gas sources 135, 136 may store precursors in a liquid phase at room temperature, which are later heated when in the gas panel 130 to convert them to a vapor-gas phase for introduction into the chamber 100. The gas sources 135, 136 may also be adapted to provide precursors through the use of a carrier gas. The gas panel 130 may be further configured to receive and then provide a purge gas from a purge gas source 138 to the process chamber 100 through the orifice 120 and the valve 125. A showerhead 160 may be coupled to the orifice 120 to deliver a process gas, purge gas, or other gas toward the wafer 190 on the support pedestal 150.

[0022] The showerhead 160 and the support pedestal 150 may serve as spaced apart electrodes for providing an electric field for igniting a plasma. A RF power source 162 may be coupled to the showerhead 160, a RF power source 163 may be coupled to the support pedestal 150, or RF power sources 162, 163 may be coupled to the showerhead 160 and the support pedestal 150, respectively. A matching network 164 may be coupled to the RF power sources 162, 163, which may be coupled to the control unit 110 to control the power supplied to the RF power sources 162, 163.

[0023] The control unit 110, such as a programmed personal computer, work station computer, and the like, may also be configured to control flow of various process gases through the gas panel 130 as well as the valve 125 during different stages of a wafer process sequence. Illustratively, the control unit 110 comprises a central processing unit (CPU) 112, support circuitry 114, and memory 116 containing associated control software 113. In addition to control of process gases through the gas panel 130, the control unit 110 may be configured to be responsible for automated control of other activities used in wafer processing---such as wafer transport, temperature control, chamber evacuation, among other activities, some of which are described elsewhere herein.

[0024] The control unit 110 may be one of any form of general purpose computer processor that can be used in an industrial setting for controlling various chambers and sub-processors. The CPU 112 may use any suitable memory 116, such as random access memory, read only memory, floppy disk drive, hard disk, or any other form of digital storage, local or remote. Various support circuits may be coupled to the CPU 112 for supporting the system 10. Software routines 113 as required may be stored in the memory 116 or executed by a second computer processor that is remotely located

(not shown). Bi-directional communications between the control unit 110 and various other components of the wafer processing system 10 are handled through numerous signal cables collectively referred to as signal buses 118, some of which are illustrated in FIG. 1.

Barrier Layer Formation

[0025] The exemplary chamber as described in Figure 1 may be used to implement the following process. Of course, other process chambers may be used. Figures 2A-2B illustrate one exemplary embodiment of barrier layer formation for fabrication of an interconnect structure in accordance with one or more aspects of the present invention.

[0026] Figure 2A is a schematic cross-sectional view of one embodiment of a substrate 200 having a dielectric layer 202 deposited thereon. Depending on the processing stage, the substrate 200 may be a silicon semiconductor wafer, or other material layer, which has been formed on the wafer. The dielectric layer 202 may be an oxide, a silicon oxide, carbon-silicon-oxide, a fluoro-silicon, a porous dielectric, or other suitable dielectric formed and patterned to provide a contact hole or via 202H extending to an exposed surface portion 202T of the substrate 200. For purposes of clarity, the substrate 200 refers to any workpiece upon which film processing is performed, and a substrate structure 250 is used to denote the substrate 200 as well as other material layers formed on the substrate 200, such as the dielectric layer 202. It is also understood by those with skill in the art that the present invention may be used in a dual damascene process flow.

[0027] Figure 2B is a schematic cross-sectional view of one embodiment of a barrier layer 204 formed over the substrate structure 250 of Figure 2A by atomic layer deposition (ALD). Preferably, the barrier layer comprises a tantalum nitride layer. Examples of other barrier layer materials which may be used include titanium (Ti), titanium nitride (TiN), titanium silicon nitride (TiSiN), tantalum (Ta), tantalum silicon nitride (TaSiN), tungsten (W), tungsten nitride (WN), tungsten silicon nitride (WSiN), and combinations thereof.

[0028] For clarity reasons, deposition of the barrier layer will be described in more detail in reference to one embodiment of the barrier layer comprising a tantalum nitride barrier layer. In one aspect, atomic layer deposition of a tantalum nitride barrier layer comprises sequentially providing a tantalum containing compound and a nitrogen

containing compound to a process chamber, such as the process chamber of Figure 1. Sequentially providing a tantalum containing compound and a nitrogen containing compound may result in the alternating chemisorption of monolayers of a tantalum containing compound and of monolayers of a nitrogen containing compound on the substrate structure 250.

[0029] Figures 3A-C illustrate one embodiment of the alternating chemisorption of monolayers of a tantalum containing compound and a nitrogen containing compound on an exemplary portion of substrate 300 in a stage of integrated circuit fabrication, and more particularly at a stage of barrier layer formation. In Figure 3A, a monolayer of a tantalum containing compound is chemisorbed on the substrate 300 by introducing a pulse of the tantalum containing compound 305 into a process chamber, such as a process chamber shown in Figure 1. It is believed that the chemisorption processes used to absorb the monolayer of the tantalum containing compound 305 are self-limiting in that only one monolayer may be chemisorbed onto the surface of the substrate 300 during a given pulse because the surface of the substrate has a finite number of sites for chemisorbing the tantalum containing compound. Once the finite number of sites are occupied by the tantalum containing compound 305, further chemisorportion of any tantalum containing compound will be blocked.

[0030] The tantalum containing compound 305 typically comprises tantalum atoms 310 with one or more reactive species 315. In one embodiment, the tantalum containing compound may be a tantalum based organo-metallic precursor or a derivative thereof. Preferably, the organo-metallic precursor is pentadimethylamino-tantalum (PDMAT; $Ta(NMe_2)_5$). PDMAT may be used to advantage for a number of reasons. PDMAT is relatively stable. PDMAT has an adequate vapor pressure which makes it easy to deliver. In particular, PDMAT may be produced with a low halide content. The halide content of PDMAT may be produced with a halide content of less than 100 ppm, and may even be produced with a halide content of less than 30 ppm or even less than 5 ppm. Not wishing to be bound by theory, it is believed that an organo-metallic precursor with a low halide content is beneficial because halides (such as chlorine) incorporated in the barrier layer may attack the copper layer deposited thereover.

[0031] The tantalum containing compounds may be other organo-metallic precursors or derivatives thereof such as, but not limited to pentaethylmethylamino-tantalum (PEMAT; $Ta[N(C_2H_5CH_3)_2]_5$), pentadiethylamino-tantalum (PDEAT; $Ta(NEt_2)_5$,), and

any and all of derivatives of PEMAT, PDEAT, or PDMAT. Other tantalum containing compounds include without limitation TBTDET ($Ta(NEt_2)_3NC_4H_9$ or $C_{16}H_{39}N_4Ta$) and tantalum halides, for example TaX_5 where X is fluorine (F), bromine (Br) or chlorine (Cl), and derivatives thereof.

[0032] The tantalum containing compound may be provided as a gas or may be provided with the aid of a carrier gas. Examples of carrier gases which may be used include, but are not limited to, helium (He), argon (Ar), nitrogen (N_2), and hydrogen (H_2).

[0033] After the monolayer of the tantalum containing compound is chemisorbed onto the substrate 300, excess tantalum containing compound is removed from the process chamber by introducing a pulse of a purge gas thereto. Examples of purge gases which may be used include, but are not limited to, helium (He), argon (Ar), nitrogen (N_2), hydrogen (H_2), and other gases.

[0034] Referring to Figure 3B, after the process chamber has been purged, a pulse of a nitrogen containing compound 325 is introduced into the process chamber. The nitrogen containing compound 325 may be provided alone or may be provided with the aid of a carrier gas. The nitrogen containing compound 325 may comprise nitrogen atoms 330 with one or more reactive species 335. The nitrogen containing compound preferably comprises ammonia gas (NH_3). Other nitrogen containing compounds may be used which include, but are not limited to, N_xH_y with x and y being integers (*e.g.*, hydrazine (N_2H_4)), dimethyl hydrazine ($(CH_3)_2N2H2$), t-butylhydrazine ($C_4H_9N_2H_3$) phenylhydrazine ($C_6H_5N_2H_3$), other hydrazine derivatives, a nitrogen plasma source (*e.g.*, N_2, N_2/H_2, NH_3, or a N_2H_4 plasma), 2,2'-azoisobutane ($(CH_3)_6C_2N_2$), ethylazide ($C_2H_5N_3$), and other suitable gases. A carrier gas may be used to deliver the nitrogen containing compound if necessary.

[0035] A monolayer of the nitrogen containing compound 325 may be chemisorbed on the monolayer of the tantalum containing compound 305. The composition and structure of precursors on a surface during atomic-layer deposition (ALD) is not precisely known. Not wishing to be bound by theory, it is believed that the chemisorbed monolayer of the nitrogen containing compound 325 reacts with the monolayer of the tantalum containing compound 305 to form a tantalum nitride layer 309. The reactive species 315, 335 form by-products 340 that are transported from the substrate surface by the vacuum system. It is believed that the reaction of the nitrogen

containing compound 325 with the tantalum containing compound 305 is self-limited since only one monolayer of the tantalum containing compound 305 was chemisorbed onto the substrate surface. In another theory, the precursors may be in an intermediate state when on a surface of the substrate. In addition, the deposited tantalum nitride layer may also contain more than simply elements of tantalum (Ta) or nitrogen (N); rather, the tantalum nitride layer may also contain more complex molecules having carbon (C), hydrogen (H), and/or oxygen (O).

[0036] After the monolayer of the nitrogen containing compound 325 is chemisorbed on the monolayer of the tantalum containing compound, any excess nitrogen containing compound is removed from the process chamber by introducing another pulse of the purge gas therein. Thereafter, as shown in Figure 3C, the tantalum nitride layer deposition sequence of alternating chemisorption of monolayers of the tantalum containing compound and of the nitrogen containing compound may be repeated, if necessary, until a desired tantalum nitride thickness is achieved.

[0037] In Figures 3A-3C, the tantalum nitride layer formation is depicted as starting with the chemisorption of a monolayer of a tantalum containing compound on the substrate followed by a monolayer of a nitrogen containing compound. Alternatively, the tantalum nitride layer formation may start with the chemisorption of a monolayer of a nitrogen containing compound on the substrate followed by a monolayer of the tantalum containing compound. Furthermore, in an alternative embodiment, a pump evacuation alone between pulses of reactant gases may be used to prevent mixing of the reactant gases.

[0038] The time duration for each pulse of the tantalum containing compound, the nitrogen containing compound, and the purge gas is variable and depends on the volume capacity of a deposition chamber employed as well as a vacuum system coupled thereto. For example, (1) a lower chamber pressure of a gas will require a longer pulse time; (2) a lower gas flow rate will require a longer time for chamber pressure to rise and stabilize requiring a longer pulse time; and (3) a large-volume chamber will take longer to fill, longer for chamber pressure to stabilize thus requiring a longer pulse time. Similarly, time between each pulse is also variable and depends on volume capacity of the process chamber as well as the vacuum system coupled thereto. In general, the time duration of a pulse of the tantalum containing compound or the nitrogen containing compound should be long enough for chemisorption of a

monolayer of the compound. In general, the pulse time of the purge gas should be long enough to remove the reaction by-products and/or any residual materials remaining in the process chamber.

[0039] Generally, a pulse time of about 1.0 second or less for a tantalum containing compound and a pulse time of about 1.0 second or less for a nitrogen containing compound are typically sufficient to chemisorb alternating monolayers on a substrate. A pulse time of about 1.0 second or less for a purge gas is typically sufficient to remove reaction by-products as well as any residual materials remaining in the process chamber. Of course, a longer pulse time may be used to ensure chemisorption of the tantalum containing compound and the nitrogen containing compound and to ensure removal of the reaction by-products.

[0040] During atomic layer deposition, the substrate may be maintained approximately below a thermal decomposition temperature of a selected tantalum containing compound. An exemplary heater temperature range to be used with tantalum containing compounds identified herein is approximately between about 20°C and about 500°C at a chamber pressure less than about 100 torr, preferably less than 50 torr. When the tantalum containing gas is PDMAT, the heater temperature is preferably between about 100°C and about 300°C, more preferably between about 175°C and 250°C. In other embodiments, it should be understood that other temperatures may be used. For example, a temperature above a thermal decomposition temperature may be used. However, the temperature should be selected so that more than 50 percent of the deposition activity is by chemisorption processes. In another example, a temperature above a thermal decomposition temperature may be used in which the amount of decomposition during each precursor deposition is limited so that the growth mode will be similar to an atomic layer deposition growth mode.

[0041] One exemplary process of depositing a tantalum nitride layer by atomic layer deposition in a process chamber, such as the process chamber of Figure 1, comprises sequentially providing pentadimethylamino-tantalum (PDMAT) at a flow rate between about 100 sccm and about 1000 sccm, and preferably between about 200 sccm and 500 sccm, for a time period of about 1.0 second or less, providing ammonia at a flow rate between about 100 sccm and about 1000 sccm, preferably between about 200 sccm and 500 sccm, for a time period of about 1.0 second or less, and a purge gas at a flow rate between about 100 sccm and about 1000 sccm, preferably between about

200 sccm and 500 sccm for a time period of about 1.0 second or less. The heater temperature preferably is maintained between about 100°C and about 300°C at a chamber pressure between about 1.0 and about 5.0 torr. This process provides a tantalum nitride layer in a thickness between about 0.5 Å and about 1.0 Å per cycle. The alternating sequence may be repeated until a desired thickness is achieved.

[0042] In one embodiment, the barrier layer, such as a tantalum nitride barrier layer, is deposited to a sidewall coverage of about 50 Å or less. In another embodiment, the barrier layer is deposited to a sidewall coverage of about 20 Å or less. In still another embodiment, the barrier layer is deposited to a sidewall coverage of about 10 Å or less. A barrier layer with a thickness of about 10 Å or less is believed to be a sufficient barrier layer to prevent copper diffusion. In one aspect, a thin barrier layer may be used to advantage in filling sub-micron and smaller features having high aspect ratios. Of course, a barrier layer having a sidewall coverage of greater than 50 Å may be used.

[0043] The barrier layer may be further plasma annealed. In one embodiment, the barrier lay may be plasma annealed with an argon plasma or an argon/hydrogen plasma. The RF power supplied to an RF electrode may be between about 100 W and about 2000 W, preferably between about 500 W and about 1000 W for a 200 mm diameter substrate and preferably between about 1000 W and about 2000 W for a 300 mm diameter substrate. The pressure of the chamber may be less than 100 torr, preferably between 0.1 torr and about 5 torr, and more preferably between about 1 torr and 3 torr. The heater temperature may be between about 20°C and about 500°C. The plasma anneal may be performed after a cycle, a plurality of cycles, or after formation of the barrier layer.

[0044] Embodiments of atomic layer deposition of the barrier layer have been described above as chemisorption of a monolayer of reactants on a substrate. The present invention also includes embodiments in which the reactants are deposited to more or less than a monolayer. The present invention also includes embodiments in which the reactants are not deposited in a self-limiting manner. The present invention also includes embodiments in which the barrier layer 204 is deposited in mainly a chemical vapor deposition process in which the reactants are delivered sequentially or simultaneously. The present invention also include embodiments in which the barrier layer 204 is deposited in a physical vapor deposition process in which the target

comprises the material to be deposited (i.e. a tantalum target in a nitrogen atmosphere for the deposition of tantalum nitride).

Process Chamber Adapted for Depositing a Seed Layer

[0045] In one embodiment, the seed layer may be deposited by any suitable technique such as physical vapor deposition, chemical vapor deposition, electroless deposition, or a combination of techniques. Suitable physical vapor deposition techniques for the deposition of the seed layer include techniques such as high density plasma physical vapor deposition (HDP PVD) or collimated or long throw sputtering. One type of HDP PVD is self-ionized plasma physical vapor deposition. An example of a chamber capable of self-ionized plasma physical vapor deposition of a seed layer is a SIP™ chamber, available from Applied Materials, Inc. of Santa Clara, California. Exemplary embodiments of chambers capable of self-ionized physical vapor deposition are described in U.S. Patent No. 6,183,614, entitled "Rotating Sputter Magnetron Assembly," which is herein incorporated by reference to the extent not inconsistent with the present invention.

[0046] Figure 4 is a schematic cross-sectional view of one embodiment of a process system 410 capable of physical vapor deposition which may be used to deposit a seed layer. Of course, other processing systems and other types of physical vapor deposition may also be used.

[0047] The process system 410 includes a vacuum chamber 412 sealed to a PVD target 414 composed of the material to be sputter deposited on a wafer 416 held on a heater pedestal 418. A shield 420 held within the chamber protects the walls of the chamber 412 from the sputtered material and provides the anode grounding plane. A selectable DC power supply 422 negatively biases the target 414 with respect to the shield 420.

[0048] A gas source 424 supplies a sputtering working gas, typically the chemically inactive gas argon, to the chamber 412 through a mass flow controller 426. A vacuum system 428 maintains the chamber at a low pressure. A computer-based controller 430 controls the reactor including the DC power supply 422 and the mass flow controllers 426.

[0049] When the argon is admitted into the chamber, the DC voltage between the target 414 and the shield 420 ignites the argon into a plasma, and the positively charged

argon ions are attracted to the negatively charged target 414. The ions strike the target 414 at a substantial energy and cause target atoms or atomic clusters to be sputtered from the target 414. Some of the target particles strike the wafer 416 and are thereby deposited on it, thereby forming a film of the target material.

[0050] To provide efficient sputtering, a magnetron 432 is positioned in back of the target 414. It has opposed magnets 434, 436 creating a magnetic field within the chamber in the neighborhood of the magnets 434, 436. The magnetic field traps electrons and, for charge neutrality, the ion density also increases to form a high-density plasma region 438 within the chamber adjacent to the magnetron 432. The magnetron 432 usually rotates about a rotational axis 458 at the center of the target 414 to achieve full coverage in sputtering of the target 414.

[0051] The pedestal 418 develops a DC self-bias, which attracts ionized sputtered particles from the plasma across the plasma sheath adjacent to the wafer 416. The effect can be accentuated with additional DC or RF biasing of the pedestal electrode 418 to additionally accelerate the ionized particles extracted across the plasma sheath towards the wafer 416, thereby controlling the directionality of sputter deposition.

Seed Layer Formation

[0052] The exemplary chamber as described in Figure 4 may be used to implement the following process. Of course, other process chambers may be used. Figure 5A-5C are schematic cross-sectional view of exemplary embodiments of depositing a seed layer over a barrier layer.

[0053] One embodiment, as shown in Figure 5A, comprises depositing a copper alloy seed layer 502 over a barrier layer 204 of Figure 2B and depositing a copper conductive material layer 506 over the copper alloy seed layer 502 to fill the feature. The term "copper conductive material layer" as used in the specification is defined as a layer comprising copper or a copper alloy. The copper alloy seed layer 502 comprises a copper metal alloy that aids in subsequent deposition of materials thereover. The copper alloy seed layer 502 may comprise copper and a second metal, such as aluminum, magnesium, titanium, zirconium, tin, other metals, and combinations thereof. The second metal preferably comprises aluminum, magnesium, titanium, and combinations thereof and more preferably comprises aluminum. In certain embodiments, the copper alloy seed layer comprises a second metal in a concentration

having the lower limits of about 0.001 atomic percent, about 0.01 atomic percent, or about 0.1 atomic percent and having the upper limits of about 5.0 atomic percent, about 2.0 atomic percent, or about 1.0 atomic percent. The concentration of the second metal in a range from any lower limit to any upper limit is within the scope of the present invention. The concentration of the second metal in the copper alloy seed layer 502 is preferably less than about 5.0 atomic percent to lower the resistance of the copper alloy seed layer 502. The term "layer" as used in the specification is defined as one or more layers. For example, for a copper alloy seed layer 502 comprising copper and a second metal in a concentration in a range between about 0.001 atomic percent and about 5.0 atomic percent, the copper alloy seed layer 502 may comprise a plurality of layers in which the total composition of the layers comprises copper and the second metal in a concentration between about 0.001 atomic percent and about 5.0 atomic percent. For illustration, examples of a copper alloy seed layer 502 comprising a plurality of layers in which the total composition of the layers comprises copper and the second metal in a concentration between about 0.001 atomic percent and about 5.0 atomic percent may comprises a first seed layer comprising the second metal and a second seed layer comprising copper, may comprise a first seed layer comprising a copper/second metal alloy and a second seed layer comprising a copper/second metal alloy, or may comprise a first seed layer comprising a copper/second metal alloy and a second seed layer comprising copper, etc.

[0054] The copper alloy seed layer 502 is deposited to a thickness of at least about a 5 Å coverage of the sidewalls of the feature or to a thickness of at least a continuous coverage of the sidewalls of the feature. In one embodiment, the copper alloy seed layer 502 is deposited to a thickness at the field areas between about 10 Å and about 2000 Å, preferably between about 500 Å and about 1000 Å for a copper alloy seed layer 502 deposited by physical vapor deposition.

[0055] Another embodiment, as shown in Figure 5B, comprises depositing a copper alloy seed layer 512 over a barrier layer 204 of Figure 2B, depositing a second seed layer 514 over the copper alloy seed layer 512, and depositing a copper conductive material layer 516 over the second seed layer 514 to fill the feature. The copper alloy seed layer 512 comprises a copper metal alloy that aids in subsequent deposition of materials thereover. The copper alloy seed layer 512 may comprise copper and a second metal, such as aluminum, magnesium, titanium, zirconium, tin, other metals,

and combinations thereof. The second metal preferably comprises aluminum, magnesium, titanium, and combinations thereof and more preferably comprises aluminum. In certain embodiments, the copper alloy seed layer comprises a second metal in a concentration having the lower limits of about 0.001 atomic percent, about 0.01 atomic percent, or about 0.1 atomic percent and having the upper limits of about 5.0 atomic percent, about 2.0 atomic percent, or about 1.0 atomic percent. The concentration of the second metal in a range from any lower limit to any upper limit is within the scope of the present invention. In one embodiment, the second seed layer 514 comprises undoped copper (i.e. pure copper). In one aspect, a second seed layer 514 comprising undoped copper is used because of its lower electrical resistivity than a copper alloy seed layer 512 of the same thickness and because of its higher resistance to surface oxidation.

[0056] The copper alloy seed layer 512 may be deposited to a thickness of less than a monolayer (i.e. a sub-monolayer thickness or a discontinuous layer) over the sidewalls of the feature. In one embodiment, the combined thickness of the copper alloy seed layer 512 and the second seed layer 514 at the field areas is between about 10 Å and about 2000 Å, preferably between about 500 Å and about 1000 Å for a copper alloy seed layer 512 and second seed layer 514 deposited by physical vapor deposition.

[0057] Another embodiment, as shown in Figure 5C, comprises depositing a first seed layer 523 over a barrier layer 204 of Figure 2B, depositing a second seed layer 524 over the first seed layer 523, and depositing a copper conductive material layer 526 over the second seed layer 524 to fill the feature. The first seed layer 523 comprises a metal selected from the group consisting of aluminum, magnesium, titanium, zirconium, tin, and combinations thereof. Preferably, the first seed layer 523 comprises aluminum. In one embodiment, the second seed layer 514 comprises undoped copper (i.e. pure copper).

[0058] The first seed layer 523 may be deposited to a thickness of less than a monolayer (i.e. a sub-monolayer thickness or a discontinuous layer) over the sidewalls of the feature. In one embodiment, the first seed layer is deposited to a thickness of less than about 50 Å sidewall coverage, preferably less than about 40 Å sidewall coverage, to lower the total resistance of the combined seed layer. The combined thickness of the first seed layer 523 and the second seed layer 524 at the field areas is between about 10 Å and about 2000 Å, preferably between about 500 Å and about

1000 Å for a first seed layer 523 and second seed layer 524 deposited by physical vapor deposition.

[0059] The copper alloy seed layer 502, 512, the first seed layer 523, or the second seed layer 514, 524 may be deposited by such techniques including physical vapor deposition, chemical vapor deposition, atomic layer deposition, electroless deposition, or a combination of techniques. In general, if a seed layer is deposited utilizing physical vapor deposition techniques, a chamber, such as the chamber 412 as described in Figure 4, includes a target, such as target 414, having a composition similar to the metal or metal alloy intended to be deposited. For example, to deposit a copper alloy seed layer 502, 512 the target may comprise copper and a second metal, such as aluminum, magnesium, titanium, zirconium, tin, other metals, and combinations thereof. The second metal preferably comprises aluminum. In certain embodiments, the target comprises a second metal in a concentration having the lower limits of about 0.001 atomic percent, about 0.01 atomic percent, or about 0.1 atomic percent and having the upper limits of about 5.0 atomic percent, about 2.0 atomic percent, or about 1.0 atomic percent. The concentration of the second metal in a range from any lower limit to any upper limit is within the scope of the present invention. In another example, to deposit a first seed layer 523, the target comprises a metal selected from the group consisting of aluminum, magnesium, titanium, zirconium, tin, and combinations thereof. If a seed layer is deposited by chemical vapor deposition or atomic layer deposition, a chamber, such as the chamber as described in Figure 1, is adapted to deliver suitable metal precursors of the metal or metal alloy to be deposited.

[0060] One exemplary process of depositing a seed layer by physical vapor deposition in a process chamber, such as the process chamber of Figure 4, comprises utilizing a target of the material to be deposited. The process chamber may be maintained at a pressure of between about 0.1 mtorr and about 10 mtorr. The target may be DC-biased at a power between about 5 kW and about 100 kW. The pedestal may be RF-biased at a power between about 0 and about 1000 W. The pedestal may be unheated (i.e. room temperature).

[0061] The copper conductive material layer 506, 516, 526 may be deposited by electroplating, physical vapor deposition, chemical vapor deposition, electroless deposition or a combination of techniques. Preferably, the copper conductive material layer 506, 516, 526 is deposited by electroplating because of the bottom-up growth

which may be obtained in electroplating processes. An exemplary electroplating method is described in United States Patent No. 6,113,771, entitled "Electro Deposition Chemistry", issued September 5, 2000, and is incorporated herein by reference to the extent not inconsistent with this invention.

[0062] It has been observed that a copper alloy seed layer, such as a copper-aluminum seed layer, has improved adhesion over a barrier layer when compared to an undoped copper seed layer over the barrier layer. Because the copper alloy seed layer has good adhesion over a barrier layer, the copper alloy seed layer acts as a good wetting agent to materials deposited thereon. Not wishing to bound by theory, it is believed that the concentration of the copper and other metals of the copper seed layer provides a seed layer with good wetting properties and good electrical characteristics. It is further believed that a copper alloy seed layer having a total thickness of less than a monolayer may be used as long as a second seed layer, such as an undoped seed layer, is deposited thereover to provide at least a combined continuous seed layer since the copper alloy seed layer provides an improved interface for adhesion of materials thereon.

[0063] Similarly, it has been observed that a metal seed layer, such as an aluminum seed layer, has improved adhesion over a barrier layer when compared to an undoped copper seed layer over the barrier layer. Because the metal seed layer has good adhesion over a barrier layer, the metal seed layer acts as a good wetting agent to materials deposited thereon. Not wishing to bound by theory, it is believed that a metal seed layer, such as an aluminum seed layer, having a total thickness of less than a monolayer may be used since the metal layer provides an improved interface for adhesion of materials thereon, such as an undoped copper seed layer deposited over the metal layer.

[0064] The seed layers as disclosed herein have improved adhesion over barrier layers and have good wetting properties for materials deposited thereover, such as a copper conductive material layer deposited thereover. Therefore, the seed layers increase device reliability by reducing the likelihood of agglomeration, dewetting, or the formation of voids in the copper conductive material layer during deposition of the copper conductive material layer, during subsequent processing at high temperatures, and during thermal stressing of the devices during use of the devices.

[0065] In one aspect, the seed layers may be used with any barrier layer and may be

used with barrier layers deposited by any deposition technique. The seed layers also may be deposited by any deposition technique. Furthermore, a conductive material layer, such as a copper conductive material layer, may be deposited over the seed layers by any deposition technique.

[0066] The present process may be used to advantage in filling apertures having less than about 0.2 micron opening width and having an aspect ratio of greater than about 4:1, about 6:1; or about 10:1.

[0067] The processes as disclosed herein may be carried out in separate chambers or may be carried out in a multi-chamber processing system having a plurality of chambers. Figure 6 is a schematic top-view diagram of one example of a multi-chamber processing system 600 which may be adapted to perform processes as disclosed herein. The apparatus is an ENDURA™ system and is commercially available from Applied Materials, Inc., of Santa Clara, California. A similar multi-chamber processing system is disclosed in U.S. Patent No. 5,186,718, entitled "Stage Vacuum Wafer Processing System and Method," (Tepman et al.), issued on February 16, 1993, where is hereby incorporated by reference to the extent not inconsistent with the present disclosure. The particular embodiment of the system 600 is provided to illustrate the invention and should not be used to limit the scope of the invention.

[0068] The system 600 generally includes load lock chambers 602, 604 for the transfer of substrates into and out from the system 600. Typically, since the system 600 is under vacuum, the load lock chambers 602, 604 may "pump down" the substrates introduced into the system 600. A first robot 610 may transfer the substrates between the load lock chambers 602, 604, processing chambers 612, 614, transfer chambers 622, 624, and other chambers 616, 618. A second robot 630 may transfer the substrates between processing chambers 632, 634, 636, 638 and the transfer chambers 622, 624. Processing chambers 612, 614, 632, 634, 636, 638 may be removed from the system 600 if not necessary for the particular process to be performed by the system 600.

[0069] In one embodiment, the system 600 is configured so that processing chamber 634 is adapted to deposit a copper alloy seed layer 502. For example, the processing chamber 634 for depositing a copper alloy seed layer 502 may be a physical vapor deposition chamber, a chemical vapor deposition chamber, or an atomic layer deposition chamber. The system 600 may be further configured so that processing

chamber 632 is adapted to deposit a barrier layer 204 in which the copper alloy seed layer 502 is deposited over the barrier layer. For example, the processing chamber 632 for depositing the barrier layer 204 may be an atomic layer deposition chamber, a chemical vapor deposition chamber, or a physical vapor deposition chamber. In one specific embodiment, the processing chamber 632 may be an atomic layer deposition chamber, such as the chamber shown in Figure 1, and the processing chamber 634 may be a physical vapor deposition chamber, such as the chamber shown in Figure 4.

[0070] In another embodiment, the system 600 is configured so that processing chamber 634 is adapted to deposit a copper alloy seed layer 512 and so that processing chamber 636 is adapted to deposit a second seed layer 514 over the copper alloy seed layer 512. For example, the processing chamber 634 for depositing a copper alloy seed layer 512 and/or the processing chamber 636 for depositing a second seed layer may be a physical vapor deposition chamber, a chemical vapor deposition chamber, or an atomic layer deposition chamber. The system 600 may be further configured so that processing chamber 632 is adapted to deposit a barrier layer 204 in which the copper alloy seed layer 512 is deposited over the barrier layer. For example, the processing chamber 632 for depositing the barrier layer 204 may be an atomic layer deposition chamber, a chemical vapor deposition chamber, or a physical vapor deposition chamber. In one specific embodiment, processing chamber 632 may be an atomic layer deposition chamber, such as the chamber shown in Figure 1, and processing chambers 634, 636 may be physical vapor deposition chambers, such as the chamber shown in Figure 4.

[0071] In another embodiment, the system 600 is configured so that processing chamber 634 is adapted to deposit a metal seed layer 523 and so that processing chamber 636 is adapted to deposit a second seed layer 524 over the metal seed layer 523. For example, the processing chamber 634 for depositing a metal seed layer 523 and/or the processing chamber 636 for depositing a second seed layer 524 may be a physical vapor deposition chamber, a chemical vapor deposition chamber, or an atomic layer deposition chamber. The system may be further configured so that processing chamber 632 is adapted to deposit a barrier layer 204 in which the metal seed layer 523 is deposited over the barrier layer. For example, the processing chamber 632 for depositing the barrier layer 204 may be an atomic layer deposition chamber, a chemical vapor deposition chamber, or a physical vapor deposition chamber. In one

specific embodiment, processing chamber 632 may be an atomic layer deposition chamber, such as the chamber shown in Figure 1, and processing chambers 634, 636 may be physical vapor deposition chambers, such as the chamber shown in Figure 4.

[0072] In one aspect, deposition of a barrier layer 204 and a seed layer (such as a copper alloy seed layer 502, a copper alloy seed layer 512 and a second seed layer 514, or a metal seed layer 523 and a second seed layer 524) may be performed in a multi-chamber processing system under vacuum to prevent air and other impurities from being incorporated into the layers and to maintain the seed structure over the barrier layer 204.

[0073] Other embodiments of the system 600 are within the scope of the present invention. For example, the position of a particular processing chamber on the system may be altered. In another example, a single processing chamber may be adapted to deposit two different layers.

EXAMPLES

Example 1

[0074] A TaN layer was deposited over a substrate by atomic layer deposition to a thickness of about 20 Å. A seed layer was deposited over the TaN layer by physical vapor deposition to a thickness of about 100 Å. The seed layer comprised either 1) undoped copper deposited utilizing a target comprising undoped copper, 2) a copper alloy comprising aluminum in a concentration of about 2.0 atomic percent deposited utilizing a copper-aluminum target comprising aluminum in a concentration of about 2.0 atomic percent, 3) a copper alloy comprising tin in a concentration of about 2.0 atomic percent deposited utilizing a copper-tin target comprising tin in a concentration of about 2.0 atomic percent, or 4) a copper alloy comprising zirconium in a concentration of about 2.0 atomic percent deposited utilizing a copper-zirconium target comprising zirconium in a concentration of about 2.0 atomic percent. The resulting substrate was annealed at a temperature of about 380°C for a time period of about 15 minutes in a nitrogen (N_2) and hydrogen (H_2) ambient.

[0075] Scanning electron microscope photographs showed agglomeration of the undoped copper layer after the anneal. The copper-zirconium alloy showed less agglomeration than the undoped copper layer. The copper-tin alloy showed less agglomeration than the copper-zirconium alloy. The copper-aluminum alloy showed no

significant agglomeration.

Example 2

[0076] Copper-aluminum alloy films comprising about 2.0 atomic percent of aluminum were deposited on different substrates by physical vapor deposition utilizing a copper-aluminum target comprising aluminum in a concentration of 2.0 atomic percent. The resulting substrates included 1) a copper-aluminum layer deposited to a thickness of about 50 Å over an ALD TaN layer, 2) a copper-aluminum layer deposited to a thickness of about 50 Å over about a 100 Å Ta layer, 3) a copper-aluminum layer deposited to a thickness of about 100 Å over an ALD TaN layer, 4) a copper-aluminum layer deposited to a thickness of about 100 Å over a silicon nitride (SiN) layer, and 5) a copper-aluminum layer deposited to a thickness of about 100 Å over a silicon oxide layer. The resulting substrates were annealed at a temperature of about 380°C for a time period of about 15 minutes in a nitrogen (N_2) and hydrogen (H_2) ambient. Scanning electron microscope photographs showed that there was no significant agglomeration of the copper-aluminum alloy over the various substrates.

Example 3

[0077] Copper-aluminum alloy films comprising about 2.0 atomic percent of aluminum were deposited by physical vapor deposition utilizing a copper-aluminum target comprising aluminum in a concentration of 2.0 atomic percent to either a 50 Å or 100 Å thickness over an ALD TaN layer. The resulting substrates were annealed at a temperature of about 380°C, about 450°C, or about 500°C for a time period of about 15 minutes in a nitrogen (N_2) and hydrogen (H_2) ambient. Scanning electron microscope photographs showed that there was no significant agglomeration of the copper-aluminum alloy for substrates annealed at temperatures of about 380°C or about 450°C. The copper-aluminum alloy showed some dewetting began to occur for substrates annealed at a temperature of about 500°C.

Example 4

[0078] Copper-aluminum alloy films comprising about 2.0 atomic percent of aluminum were deposited by physical vapor deposition utilizing a copper-aluminum target comprising aluminum in a concentration of about 2.0 atomic percent to either about a

50 Å or about a 100 Å thickness over an ALD TaN layer. The resulting substrates were annealed at a temperature of about 450°C for a time period of about 30 minutes in a nitrogen (N_2) and hydrogen (H_2) ambient. Scanning electron microscope photographs showed that there was no significant agglomeration of the copper-aluminum alloy for substrates annealed at a temperature of about 450°C for a time period of about 30 minutes.

[0079] While foregoing is directed to the preferred embodiment of the present invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.